

Introduction to Computer Architecture and Organization

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(A concise, easy-to-read study guide)

1. What Is Computer Architecture?

Aspect	Definition
Architecture	The <i>visible</i> attributes of a system that affect programming: instruction set, memory hierarchy, I/O mechanisms, addressing modes, and system-level performance goals.
Organization	The <i>implementation</i> details that realize the architecture: datapath design, control logic, micro-operations, pipelines, cache structures, and physical interconnects.
Key Idea	Architecture = <i>what</i> the computer does. Organization = <i>how</i> it does it.

2. Levels of Design (From High-Level to Low-Level)

- High-Level Architecture** – Instruction Set Architecture (ISA)
- Micro-Architecture** – Datapath & control unit design
- Logic Implementation** – Gate-level circuits, RTL (Register Transfer Language)
- Physical Implementation** – Chip layout, floorplanning, packaging

(Each lower level must satisfy the specifications of the level above it.)

3. Instruction Set Architecture (ISA)

Category	Examples	Why It Matters
Data Types	Integer, floating-point, SIMD vectors, packed BCD	Determines operand size & precision.
Instruction Formats	R-type, I-type, J-type (MIPS); VEX prefix (x86)	Defines encoding, length, and decoding complexity.
Addressing Modes	Register, immediate, base+offset, PC-relative, indexed	Impacts code density and compiler optimization.

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Category	Examples	Why It Matters
Control Flow	Branch, jump, call/return, conditional move	Influences pipeline hazards & branch prediction.
Privilege Levels	User, kernel (ring 0), hypervisor	Provides security & isolation.
Exceptions & Interrupts	Fault, trap, abort, system call	Enables OS interaction and error handling.

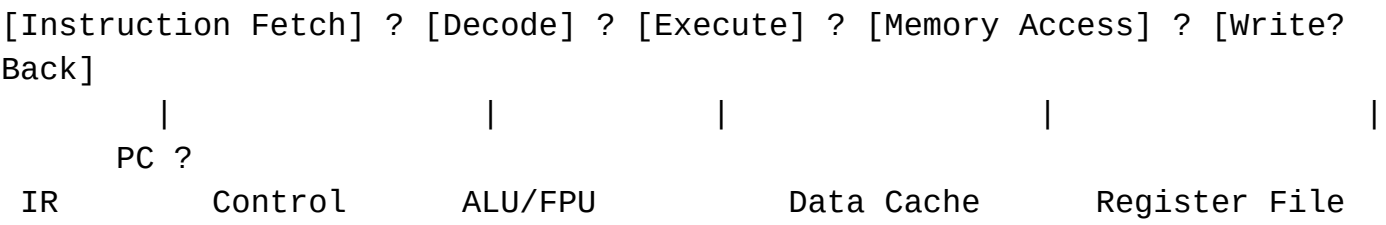
Common ISAs: x86-64, ARMv8-A, RISC-V, MIPS, PowerPC.

4. Basic Computer Organization

4.1. Central Components

Component	Function
ALU (Arithmetic Logic Unit)	Executes integer/floating-point arithmetic, logical ops, shifts.
Registers	Fast, on-chip storage for operands, results, control info (e.g., PC, IR, status flags).
Control Unit	Generates control signals; can be <i>hardwired</i> or <i>microprogrammed</i> .
Memory Hierarchy	Registers ? L1/L2/L3 caches ? Main memory (DRAM) ? Secondary storage.
I/O Subsystem	Device controllers, buses, interrupt handling.
Clock	Global timing reference; defines cycle time (period).

4.2. Data Path Overview



The classic **5-stage pipeline** (IF, ID, EX, MEM, WB) is the foundation of many modern CPUs.

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5. Memory System

Level	Typical Size	Latency (cycles)	Purpose
Registers	32–256?KB (total)	1	